

Appl. No. 10/815,484
Amdt. Dated 08/28/2006
Reply to Office Action of May 26, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus adapted to a digital device, comprising:
core logic;
a first conditional access (CA) logic block connected to the core logic, the first CA logic block using a first CA function associated with a first CA provider; and
a second CA logic block connected to the core logic, the second CA logic block using a second CA function associated with a second CA provider,
wherein a connection between the core logic and the first CA logic block is disabled when descrambling of the incoming scrambled content is to be conducted according to the second CA function.
2. (Original) The apparatus of claim 1 is a CableCARD coupled to a set-top box.
3. (Original) The apparatus of claim 1, wherein the core logic comprising:
a processor core;
a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key; and
a non-volatile memory accessible by the processor core, the non-volatile memory to contain information in a scrambled format, the information being recovered using the key contained in the secure non-volatile memory.
4. (Original) The apparatus of claim 3, wherein the core logic further comprises a descrambler shared by the first CA logic block and the second CA logic block to descramble the incoming data.
5. (Original) The apparatus of claim 3, wherein each of the first CA logic block and the second CA logic block further comprises a descrambler to descramble the incoming data.

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6. (Original) The apparatus of claim 3, wherein the core logic further comprises a metal shield surrounding the processor core, the secure non-volatile memory and the non-volatile memory, the shield being made of a conductive material over which power is supplied to the secure non-volatile memory.

7. (Original) The apparatus of claim 6, wherein the key is erased from the secure non-volatile memory if a supply of power is disrupted to the secure non-volatile memory due to tampering of the shield.

8. (Original) The apparatus of claim 1, wherein the first and second CA logic blocks are one-time programmable logic devices.

9. (Original) The apparatus of claim 1, wherein the first and second CA logic blocks are field programmable gate arrays.

10. (Original) The apparatus of claim 1, wherein the first CA function differs from the second CA function.

11. (Original) An apparatus adapted to a digital device, comprising:
core logic; and

a plurality of conditional access logic blocks coupled to the core logic and including a first conditional access logic block and a second conditional access logic block, the first conditional access logic block using a first conditional access (CA) function associated with a first CA provider and the second conditional access logic block using a second CA function associated with a second CA provider,

wherein enabling only the first conditional access logic block of the plurality of conditional access logic blocks when the incoming scrambled content is scrambled according to the first CA function.

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12. (Original) The apparatus of claim 11, wherein the core logic further comprises a descrambler shared by the plurality of conditional access logic blocks to descramble the incoming data.

13. (Original) The apparatus of claim 11, wherein each of the plurality of conditional access logic blocks further comprises a descrambler to descramble the incoming data.

14. (Original) The apparatus of claim 11, wherein each of the plurality of conditional access logic blocks is a field programmable gate array.

15. (Original) The apparatus of claim 11, wherein each of the plurality of conditional access logic blocks is a one-time programmable logic device.

16. (Original) The apparatus of claim 15, wherein each of the plurality of conditional access logic blocks is battery-backed so that disruption of power will cause all of the plurality of conditional access logic blocks to become inoperative.

17. (Original) The apparatus of claim 11, wherein each of the plurality of conditional access logic blocks is a programmable logic device including programmable gates that are programmed at every power-up.

18. (Original) The apparatus of claim 17, wherein the core logic comprises:
a battery-backed, non-volatile memory to contain a descrambling key; and
a descrambler coupled to the battery-backed non-volatile memory, the descrambler using the descrambling key to program the programmable gates of each of the plurality of conditional access logic blocks.

19. (Original) The apparatus of claim 11 being a network card connected to a set-top box.

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20. (Currently Amended) An apparatus adapted for coupling to internal circuitry of a digital device and for descrambling incoming scrambled content, comprising:

core logic; and

a programmable logic device including a plurality of programmable gates programmed to operate in accordance with a conditional access (CA) function associated with a first CA provider to descramble the incoming scrambled content, the programmable gates of the programmable logic device are one-time programmable and battery-backed so that disruption of power will cause the programmable logic device to become inoperative.

21. (Cancelled).

22. (Original) The apparatus of claim 20, wherein the core logic comprising:

a processor core;

a secure non-volatile memory accessible by the processor core, the secure non-volatile memory to contain a key;

a non-volatile memory accessible by the processor core, the non-volatile memory to contain information in a scrambled format, the information being recovered using the key contained in the secure non-volatile memory; and

a shield adapted to cover the processor core, the secure non-volatile memory and the non-volatile memory, the shield being made of a conductive material over which power is supplied to the secure non-volatile memory.

23. (Original) The apparatus of claim 20, wherein the programmable gates of the programmable logic device are programmed at every power-up.